



The Road Ahead: Intel® Itanium® Architecture and Software

Don Soltis - Senior Principal Engineer
James Reinders - Director
Intel Corporation

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Gelato ICE April 2006



Itanium® Processor Target Markets

RISC replacement, Commercial and Technical

- SMP - 2 way to 512 way today
- Cluster
- Front end servers with virtualization

High reliability

- Increased detection and correction

Multiple OS & system vendors

- Windows*, Linux*, HP-UX*, OpenVMS*, NonStop*

>7000 apps

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Itanium® Processor Platform Support

Users



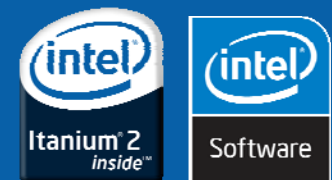
Applications



OS Vendors



System Vendors



Itanium[®] Processor Roadmap

Processor
Generation

Highlights

New
Technologies

Targeted Line
Items for RISC
Replacement

Availability

Processor Generation	Itanium 2 Processor (Madison 9M/ Fanwood)	Montecito	Montvale	Tukwila	Poulson
Highlights	9MB cache, faster FSB	Dual-core, HT, 24MB cache	Enhanced dual-core architecture	Multi-core	Enhanced multi-core architecture
New Technologies	<ul style="list-style-type: none"> • EPIC • Machine Check Architecture • Advanced register model • Large address space 	<ul style="list-style-type: none"> • Dual-core • Hyper-Threading Technology • Intel[®] Virtualization Technology • Enhanced cache reliability (Pellston) • Enhanced data integrity (Lockstep) 		<ul style="list-style-type: none"> • Multi-core • High speed system interconnects • Common platform architecture with Intel[®] Xeon[™] processor MP • Enhanced RAS • Enhanced virtualization • Enhanced I/O & memory 	
Targeted Line Items for RISC Replacement			Enterprise HPC Ultra dense		
Availability	2005	2006	2007	2008	Future

Product dates and features subject to change without notice.

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Intel® Software Development Products

Itanium®



1999-2001

Itanium 2

Improved Performance
New Arch.
Feature Support

Threading Tools

Expanded Linux*
Support



2002-2003

Itanium 2

More Performance

OpenMP*
for clusters

MPI library

Multi-core support



2004-2005

Montecito

Performance tuned for
New Arch.

VTune™ Analyzer
IPF features incl. native GUI

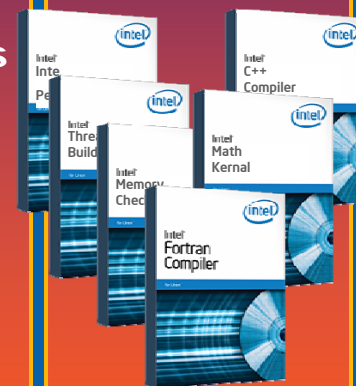
Memory Checker

Added Models /
Support for parallelism

2006

Beyond Montecito

Performance & New Features



and more based on
customer feedback...

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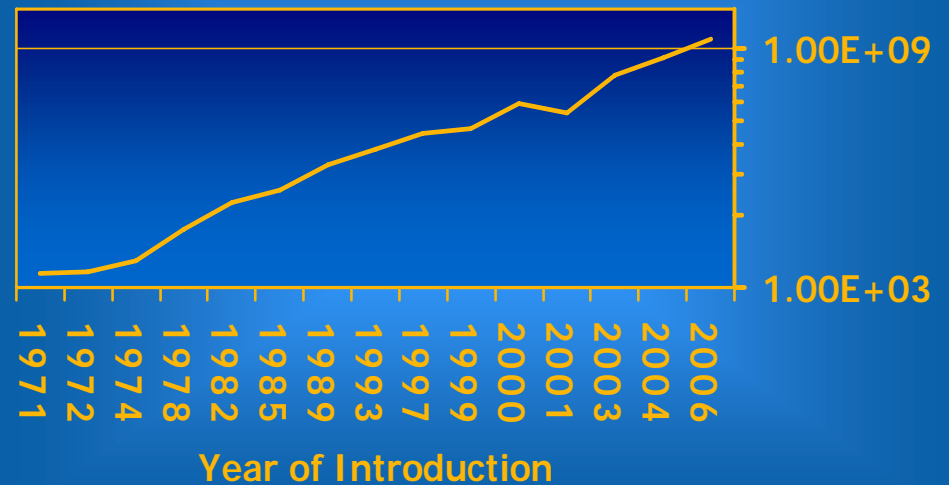


Technology Trends

What to do with all those transistors?

- More cores
- Memory controllers
- Platform component integration
- H/W acceleration
- System bandwidth

Processor Transistors



Increased level of parallelism per socket and per system

- S/W support - Scalability, correctness, ease of programming
- H/W support - Bandwidth, reliability, partitioning

Hardware Performance Features

Robust performance across variety of applications

- Single threaded
- Throughput
- Technical: Floating Point, Integer, Cryptography

Built with system level focus

Scalable

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Multi-core Software Support

Use of multiple processors, very important to us and our customers

Three key challenges:

- Scalability
- Correctness
- Ease of programming

Multi-Platform Software Support

Scale



we ♥ MPI

- Ste

- MPI - highly scalable

- OpenMP* - scalable



we ♥ OpenMP

We help make it easier



Multi-core Software Support

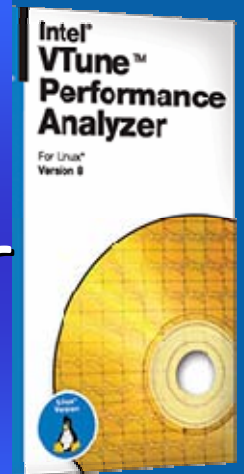
Correctness

- How will we help more developers use parallelism?



Intel® Thread Checker
pinpoints latent threading errors

Intel® Thread Profiler
Intel® VTune™ Performance Analyzer
two ways to gain
precise insight into threaded
code – application/lock level
or application/system level



We help make it easier

Put Thread Safety In *Your* Development Cycle

Simplify the creation and debugging of
scalable thread safe code

- Patented advanced error detection engine identifies latent data races and deadlocks
- Command line interface provides a scriptable interface for easy integration into your testing environment
- Native Linux* support through command line views utilizing source instrumentation



Join the beta program -
www.intel.com/software/products/threading/beta

Visit the Intel booth

Can we make it easier still?

- Porting algorithms and data structures to work in parallel can be difficult
- Would a tool that provides a new approach that makes this easier be worthwhile?

we think so



The Next Parallel Programming Model

first public mention
you are invited to join our beta

C++ template-based runtime library

- simplifies writing multi-threaded applications
- high level programming paradigm
- emphasizes scalability
- pre-built and tested data structures & algorithms

Join the parallel programming beta:
www.intel.com/software/products/tbb/beta

SEE A DEMO
Visit the Intel booth

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RISC / Mainframe Class Reliability

- Data integrity
 - Error coverage across key elements of the processor
 - caches, TLB, FSB
 - Montecito extends coverage to registers and hard errors in L3 cache, and adds lockstep support
 - Future processors will continue to augment
- High availability
 - Smooth error detection, correction, recovery and containment enabled by advanced Machine Check Architecture
 - Integrated platform error handling through hardware-firmware- OS partnership
- Comprehensive platform RAS
 - Enterprise leaders deliver comprehensive RAS capabilities for Itanium® platforms
 - Hard partitions, memory scrubbing, memory sparing, redundancy, hot swapping, and more

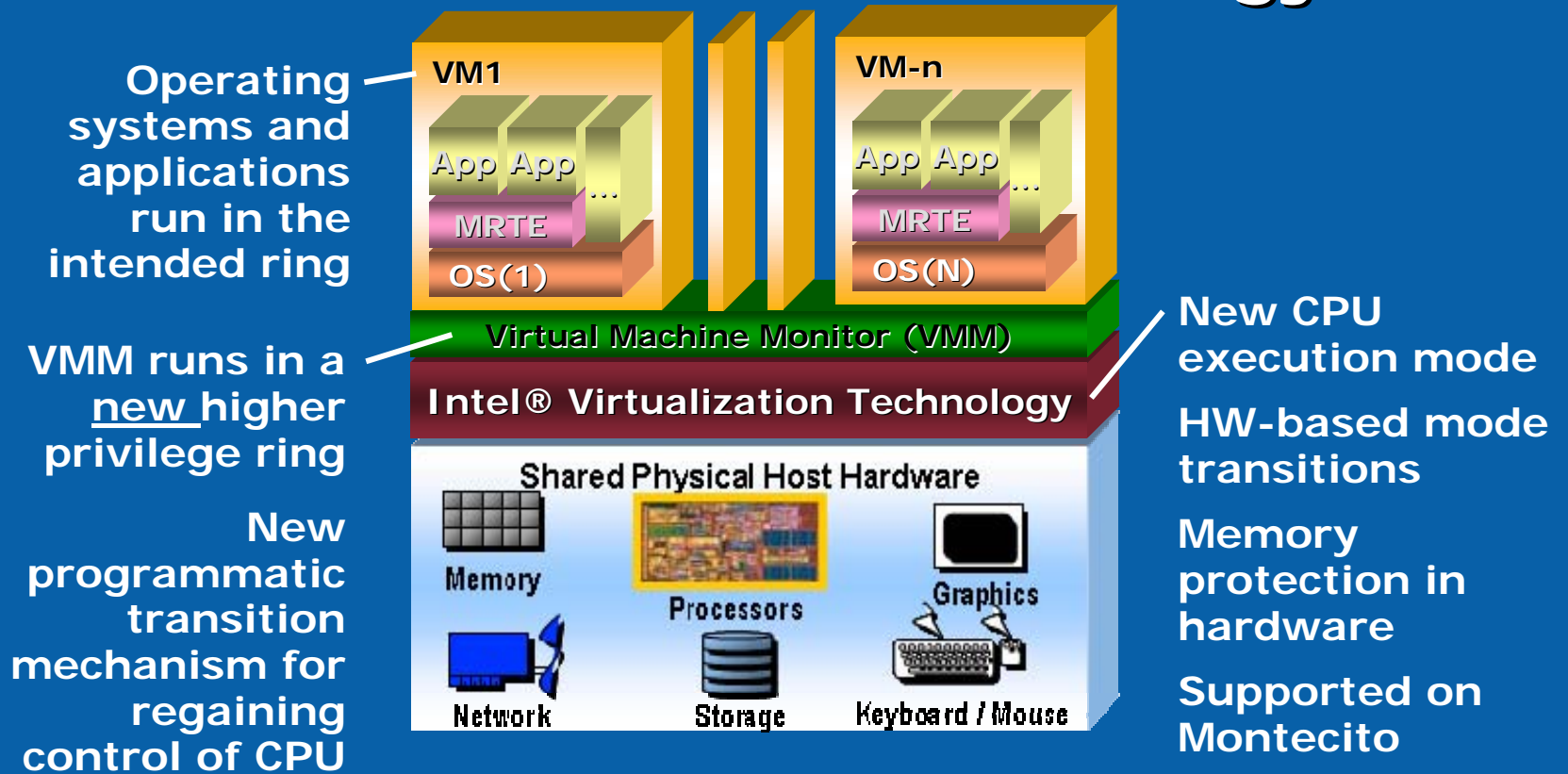
L1 cache/ tags	Parity
L2 cache/ tags	ECC
L3 cache/ tags	ECC
Registers	Parity
TLB	Parity
FSB	ECC

Extensive Error Coverage¹



¹ Error coverage shown is for Montecito. Register coverage includes integer, floating point, and branch prediction.

Intel® Virtualization Technology



VT eliminates virtualization holes and need for unorthodox software methods while enabling VMMs to become independent of guest OS

Reliability Is A Software Concern Too

During the Gelato 2005 ICE,
a memory checker
was frequently requested

We are Listening



beta release of
VTune™ Performance Analyzer
with the Memory Checker
first public mention

Technology Preview of our Memory Checker is included with the VTune™ Analyzer beta for Itanium® Processors

- Multi-threaded and multi-processor support
- all the *technology* is there now, GUI coming, full product announcement later this year

Intel® VTune™ Performance Analyzer *you are invited to join our beta*

VTune Analyzer includes major enhancements for support of Intel Itanium® 2 processors

Intel is providing CD-ROMs of beta release to Gelato attendees that *includes* our Memory Checker at the Intel booth

Attend Jasper Kamperman's Session, 11:15 am, Siskiyou Room: "Dynamic Instrumentation-Based System for Building Tools"

Get the beta at the Intel booth or email vtune_beta@intel.com

Summary

- Itanium® processors are the foundation of great platforms
 - Our processors have an exciting roadmap ahead including multi-core, virtualization while maintaining performance and high reliability
 - Industry support is tremendous, and our key to success
 - We understand the needs which multi-core and reliability concerns bring – and lead with our software to help address the needs
 - Come visit us in the Intel booth



More Information

- Itanium® 2 processor product information
 - intel.com/products/processor/itanium2/index.htm
- Itanium architecture benefits
 - intel.com/business/bss/products/server/itanium2/index.htm
- Case studies and solution blueprints
 - mysearch.intel.com/bizcontent/default.aspx?contentType=cs
- Itanium Solutions Alliance*
 - www.itaniumsolutionsalliance.org
- Gelato* – advancing Linux* on Itanium architecture
 - www.gelato.org
- Mission-critical Infrastructure Resource Center
 - itanium.techweb.com
- Intel® Software Development Products
 - www.intel.com/software/products



Thank You

